UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,026	08/14/2000	Paul A. Farrar	M4065.0082/P082-A	8833

24998 7590 08/24/2004

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/638,026
Filing Date: August 14, 2000
Appellant(s): FARRAR, PAUL A.

Thomas J. D'Amico
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04-15-04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 40, 43-51, 68-72, 74 and 75 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of the claims under appeal.

5,925,931	Yamamoto	07-1999
5,249,347	Svetkoff et al.	06-2001
5,888,884	Wojnarowski	03-1999
(Japanese Pat. 408,236,938)	Takashi et al.	09-1996
Admitted Prior Art (APA)		

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

I. Claims 40, 43-49, 68, 71, 72, 74 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) in view of Svetkoff et al. (US Pat. 6249347).

Regarding claim 40, Yamamoto discloses a semiconductor device/an integrated circuit (IC) chip on a semiconductor substrate/silicon wafer (21/22 in Fig. 7) comprising:

- a semiconductor structure having a metal contact (23 in Fig. 7) formed on the surface thereof
- a first insulator layer (24/41 in Fig. 7) overlying the metal contact
- a metal pad/interconnection (50 in Fig. 7) overlying the first insulator layer and in contact with the metal contact, the metal pad being partially overtop of the metal contact and comprising a stack of three different metals/levels including zinc or nickel, copper and gold (see 46A, 46B and 50 in Fig. 4 and 7; Col. 5, lines 9-35)
- a second insulator layer (47 in Fig. 7) overlying the metal pad
- the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) in the first insulator, and
- solder contact/ball (48 in Fig. 7) formed in the second insulator layer and in contact with the metal pad, the solder contact/ball extending from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (Fig. 7)

(Fig. 7; Col. 6, line 40- Col. 7, line 5; Col. 4-8).

Yamamoto fails to teach the diameter of the solder contact being less than 100 microns.

Svetkoff et al. teach a miniature/micro ball grid array (BGA) device using solder balls (200 in Fig. 11) having a typical range of 10-300 microns to achieve the increased interconnect density and very fine geometries/ground rules (Col. 11, lines 27-37; Col. 1 and 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device.

Regarding claims 43 and 44, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40, except the solder contacts having the diameter of less than 10 microns or that being approximately 2 microns respectively.

The determination of parameters such as size/dimension, range and shape of the metal/solder contacts and metallization structure including diameter, pitch/spacing, pad dimension, number/thickness of an insulating layer, number/diameter of vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired I/O density, line width/ground rules, performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 10

microns, approximately 2 microns or having a range of 2-100 microns as taught by Svetkoff et al. so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device.

Regarding claim 45, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) formed in the first insulator.

Regarding claim 46, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the solder contacts being extended from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (see Fig. 7).

Regarding claim 47, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the metal pad being partially overtop of the metal contact (see Fig. 7).

Regarding claim 48, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teaches the semiconductor device being the IC chip (21/22 in Fig. 7).

Regarding claim 49, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, including the semiconductor device being an IC wafer (21/22 in Fig. 7).

Regarding claim 68, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, except the first insulating layer being 2 microns thicker than the metal contact.

Yamamoto further teaches the first insulating layer being 10-50 microns thick (41 in Fig. 7; Col. 4, line 39) and as shown in Fig. 7, the insulating layer being approximately 2-3 times thicker than the metal pad/contact (23 in Fig. 7) or more than 2 microns thicker than the metal pad/contact.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. and the first insulating layer being 2 microns thicker than the metal contact so that the interconnect density and passivation/insulation integrity can be improved in Yamamoto's device.

Regarding claim 71, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter between 2-100 microns.

Regarding claim 72, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of approximately 2 microns.

Regarding claim 74, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of less than 50 microns.

Regarding claim 75, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of less than 25 microns.

II. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) and Svetkoff et al. (US Pat. 6249347) as applied to claim 40 above, and further in view of the admitted prior art (APA).

Regarding claims 50 and 51, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, except the device being bonded to a module substrate or a circuit board respectively.

APA teaches a semiconductor device being bonded to a module substrate or a circuit board (specification page 2; Fig. 1-3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. and the device being bonded to the module substrate as taught by APA so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto and Svetkoff et al's device.

III. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) and Svetkoff et al. (US Pat. 6249347) as applied to claim 40 above, and further in view of Wojnarowski (US Pat. 5888884).

Regarding claim 69, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the metal pad comprising three different metals, but Yamamoto and Svetkoff et al. fail to teach the metal pad comprising a stack comprising four different metal levels.

Wojnarowski teaches a device having a pad metallization comprising four or more metal layers/levels comprising an aluminum (40 in Fig. 5-8; Col. 6, line 41), chromium, titanium or nickel-titanium (Col. 7, line 41) and one or more layers/levels of different metals including gold, copper, platinum, etc. (Col. 7, lines 43-46) to provide an improved adhesion and diffusion barrier (Col. 7, lines 36-46).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal pad comprising a stack comprising four

different metal levels as taught by Wojnarowski so that the adhesion, bonding and reliability of metallization can be improved in Yamamoto and Svetkoff et al's device.

IV. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931), Svetkoff et al. (US Pat. 6249347) and Wojnarowski (US Pat. 5888884) as applied to claims 40 and 69 above, and further in view of Takashi et al. (Japanese Pat. 408236938).

Regarding claim 70, Yamamoto, Svetkoff et al. and Wojnarowski teach substantially the entire claimed structure as applied to claims 40 and 69 above, except the metal stack comprising zirconium as one of the four metals in the stack.

Takashi et al. teach using metal pad/conductor (114 in Fig. 1-4) comprising metals/alloys comprising metal such as zirconium (see abstract in English Translation).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal stack comprising zirconium as one of the four metals as taught by Takashi et al. so that the desired electrical parameters/properties of the metallization can be achieved and the reliability of the interconnection can be improved Yamamoto, Svetkoff et al. and Wojnarowski's device.

(11) Response to Arguments

I. Rejection of claims 40, 45-51, 68 and 71:

Appellant presents following arguments:

A. Svetkoff et al. cannot be combined with Yamamoto because Svetkoff et al. do not relate to solder contacts and Svetkoff et al. imaging system is not analogous to the semiconductor device of the present invention, and

B. Svetkoff et al. do not teach how to make or use the semiconductor device with the solder balls in the range of 2-300 microns.

A. Svetkoff et al. clearly discloses the objectives of the invention to provide imaging requirements for semiconductor industry including measurement, detection and characterization of height/diameter of an array of micro-ball grid array (BGA) solder balls/contacts (Col. 2, lines 1-17). Such array having 10-300 micron diameter solder balls and interconnects having very fine geometries (1-3 microns height) is used in wafer scale semiconductor technology and a variety of other sub-micron measurement applications (Col. 5, lines 40-45; Col. 11, lines 27-36; Col. 1 and 2). The array showing such micro-BGA contacts in a semiconductor device shown in Fig. 11, is commonly found in the semiconductor industry (Col. 11, lines 28-36). Examiner holds that Svetkoff et al's teaching is pertinent to problems and the characterization of micro-BGA contacts, solder joints and interconnects on the semiconductor device.

See In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992).

B. Regarding appellant's arguments about the diameter of the solder contacts being in the range of 2-300 microns, Svetkoff et al. teach the miniature/micro BGA device with the solder balls having a diameter in a typical range of 10-300 microns to achieve the increased interconnect density and very fine geometries/ground rules (Col. 11, lines 27-37; Col. 1 and 2). The determination of parameters such as size/dimension, range and shape of the metal/solder contacts and metallization structure including diameter, pitch/spacing, pad dimension, number/thickness of an insulating layer, number/diameter of vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired interconnect density, line width/ground rules and device performance. It would have been obvious to an artisan to arrive at a solder contact dimension being less than 10, 25 or 50 microns, approximately 2 microns or having a range of 2-100 microns so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device. See In re Aller, 105 USPQ 233.

Furthermore, regarding the appellant's argument about Svetkoff et al. not disclosing the method of making the device/die having solder contacts having less than 100 microns diameter, it seems that appellant did not consider examiner's explanation as previously stated in the final action (paper no. 19, dated 01-15-04) that the claims of the invention are directed to the semiconductor device/structure comprising the micro solder contacts and not a method of making such contacts.

II. Rejection of claims 74 and 75:

Appellant's arguments regarding the diameter of the solder contacts being less than 50 or 25 microns respectively have been addressed in the item I above.

III. Rejection of claim 43:

Appellant's arguments regarding the diameter of the solder contacts being less than 10 microns have been addressed in the item I above.

IV. Rejection of claims 44 and 72:

Appellant's arguments regarding the diameter of the solder contacts being approximately 2 microns have been addressed in the item I above.

V. Rejection of claim 69:

Appellant argues that Wojnarowski discloses a single barrier layer and a single conducting metal layer, or at most three metal levels, but do not disclose the metal pad comprising the metal stack comprising four different metal levels.

Wojnarowski teaches a device having a pad metallization comprising a metal layer comprising an aluminum (40 in Fig. 5-8; Col. 6, line 41), an adhesion/barrier layer of chromium (Cr), titanium (Ti), titanium- tungsten (TiW) or nickel-chromium/Ni-Cr (Col. 7, line 41) followed by a conducting metal layer of one or more different metals including gold (Au), copper (Cu), platinum (Pt), aluminum (Al), tungsten (W), etc. (Col. 7, lines 43-

46). Such conducting metal layer of one or more different metals would form a laminated or a stacked metal layer on the underlying adhesion/barrier layer and aluminum layer. It would have been obvious to an artisan to realize that such combination of laminated/stacked conducting metal layer on top of aluminum and the adhesion/barrier layer would form a stack comprising four different metal levels.

VI. Rejection of claim 70:

Appellant argues that Takashi et al. disclose the metal pad layer being applied as copper-zirconium alloy and not as zirconium as claimed.

However, the metal alloy in Takashi et al's pad comprises the copper-zirconium (see English Translation, constitution: line 13), which comprises the zirconium.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

NP
August 17, 2004

Appeal Conferees

BRIAN SIRQUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Conferees

Brian Sircus

Eddie Lee

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Nitin Parekh

THOMAS J. D'AMICO
C. DONALD STEVENS
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526